

What is claimed:

1        1. A method for manufacturing a semiconductor device, the semiconductor  
2 device having a DRAM including a cell capacitor formed in a DRAM region of a  
3 semiconductor substrate, and a capacitor element formed in an analog element region of the  
4 semiconductor substrate, the method comprising the steps of:

5                (a) simultaneously forming a bit line that is a component of the DRAM and a  
6 connection layer that is located in a common layer with the bit line and this is used to  
7 electrically connect a lower electrode of the capacitor element and another semiconductor  
8 element;

9                (b) simultaneously forming a storage node of the cell capacitor and the lower  
10 electrode;

11                (c) simultaneously forming a dielectric layer of the cell capacitor and a dielectric  
12 layer of the capacitor element; and

13                (d) simultaneously forming a cell plate of the cell capacitor and an upper electrode  
14 of the capacitor element.

1        2. A method for manufacturing a semiconductor device according to claim 1,  
2 further comprising the step of:

3                (e) forming a first resistance element and a second resistance element in the analog  
4 element region,

5                wherein the step (e) is carried out simultaneously with the step (d), and  
6                wherein a number of ion-implantations of impurity in a region where the first  
7 resistance element is to be formed is greater than a number of ion-implantation of impurity  
8 in a region where the second resistance element is to be formed so that a resistance value of  
9 the first resistance element is lower than a resistance value of the second resistance element.

1       3.     A method for manufacturing a semiconductor device according to claim 1,  
2 further comprising the step of:

3       (e) forming a first resistance element and a second resistance element in the analog  
4 element region,

5       wherein the step (e) is carried out simultaneously with the step (d), and

6       wherein an impurity is diffused in a region where the first resistance element is to be  
7 formed so that a resistance value of the first resistance element is lower than a resistance  
8 value of the second resistance element.

1       4.     A method for manufacturing a semiconductor device according to claim 1,  
2 further comprising the step of:

3       (e) forming a first resistance element and a second resistance element in the analog  
4 element region,

5       wherein the step (e) is carried out simultaneously with the step (d), and

6       wherein a silicide layer is formed in a region where the first resistance element is to  
7 be formed so that a resistance value of the first resistance element is lower than a resistance  
8 value of the second resistance element.

1       5.     A semiconductor device having a DRAM including a cell capacitor formed in  
2 a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog  
3 element region of the semiconductor substrate, the semiconductor device comprising:

4       an interlayer dielectric layer, an embedded connection layer and a connection layer,  
5       wherein the interlayer dielectric layer is located between the semiconductor substrate  
6 and the capacitor element,

7       the connection layer and the embedded connection layer are used to electrically  
8 connect a lower electrode of the capacitor element to another semiconductor element,

9       the connection layer is located in a common layer of a bit line that is a component of  
10 the DRAM,

11       the embedded connection layer is located in a connection hole formed in the  
12 interlayer dielectric layer,

13        one end of the embedded connection layer connects to the lower electrode at a  
14      bottom surface of the lower electrode, and  
15        another end of the embedded connection layer connects to the connection layer.

1        6.      A semiconductor device according to claim 5, further comprising  
2        an additional capacitor element,  
3        wherein the additional capacitor element is located in the analog element region, and  
4        the capacitor element and the additional capacitor element are serially connected to  
5        each other by the embedded connection layer and the connection layer.

1        7.      A semiconductor device according to claim 5, further comprising a first  
2        resistance element and a second resistance element,  
3        wherein the first resistance element and the second resistance element are located in  
4        the analog element region, and  
5        an impurity concentration of the first resistance element is higher than an impurity  
6        concentration of the second resistance element so that a resistance value of the first  
7        resistance element is lower than a resistance value of the second resistance element.

1        8.      A semiconductor device according to claim 6, further comprising a first  
2        resistance element and a second resistance element,  
3        wherein the first resistance element and the second resistance element are located in  
4        the analog element region, and  
5        an impurity concentration of the first resistance element is higher than an impurity  
6        concentration of the second resistance element so that a resistance value of the first  
7        resistance element is lower than a resistance value of the second resistance element.

1        9.    A semiconductor device according to claim 5, further comprising a first  
2 resistance element and a second resistance element,

3            wherein the first resistance element and the second resistance element are located in  
4 the analog element region, and

5            the first resistance element includes a silicide layer so that a resistance value of the  
6 first resistance element is lower than a resistance value of the second resistance element.

1        10.   A semiconductor device according to claim 6, further comprising a first  
2 resistance element and a second resistance element,

3            wherein the first resistance element and the second resistance element are located in  
4 the analog element region, and

5            the first resistance element includes a silicide layer so that a resistance value of the  
6 first resistance element is lower than a resistance value of the second resistance element.

1        11.   A semiconductor device according to claim 5, wherein a thickness of a  
2 dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of  
3 the cell capacitor.

1        12.   A semiconductor device according to claim 6, wherein a thickness of a  
2 dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of  
3 the cell capacitor.

1        13.   A semiconductor device according to claim 7, wherein a thickness of a  
2 dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of  
3 the cell capacitor.

1        14.   semiconductor device according to claim 9, wherein a thickness of a  
2 dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of  
3 the cell capacitor.

1        15. A method for manufacturing a semiconductor device, the semiconductor  
2 device having a DRAM including a cell capacitor formed in a DRAM region of a  
3 semiconductor substrate, and a capacitor element formed in an analog element region of the  
4 semiconductor substrate, the method comprising:

5                forming a first conducting layer and etching a portion of the first conducting layer to  
6 form a bit line that is a component of the DRAM and a connection layer that is located in a  
7 common layer with the bit line and used to electrically connect a lower electrode of the  
8 capacitor element and another semiconductor element;

9                forming a second conducting layer and etching a portion of the second conducting  
10 layer to form a storage node of the cell capacitor and the lower electrode;

11               forming a dielectric layer and etching a portion of the dielectric layer to form a  
12 dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

13               forming a third conducting layer and etching a portion of the third conducting layer  
14 to form a cell plate of the cell capacitor and an upper electrode of the capacitor element.

1        16. A method according to claim 15, further comprising forming a first resistance  
2 element and a second resistance element in the analog element from the third conducting  
3 layer, wherein the first resistance element and second resistance element are formed so that a  
4 resistance value of the first resistance element is lower than a resistance value of the second  
5 resistance element.